AN3276
Application note

ST solution for efficiency improvement in PFC applications, back current circuit (BC^2)

Introduction

The challenges for modern high efficiency switching power supplies are to minimize power losses and increase their power density without raising the cost. The goal is to reduce both power conduction and power switching losses.

Minimization of power conduction losses is difficult to achieve without considerably affecting the cost and power density, since more material is required (bigger active and passive components). Unlike the conduction losses, it is easier to reduce the power switching losses without significantly increasing the power supply cost. There are two main ways to achieve this improvement:

- working on the dynamic behavior of the semiconductor technologies
- working on circuit topologies

Novel diodes using technologies such as SiC and GaN materials significantly reduce the switching losses. However, their high price makes them not so attractive for applications such as desktop server power supplies, solar inverters and µinverters.

The patented circuit [see *Section 5: References*, *1.*], described in this Application note is based on the soft switching method and meets market expectations since its efficiency/cost/power, and density/EMI trade-offs are better than high voltage SiC Schottky diodes.

Contents

1 **Existing solutions 3**

1.1 Diode switch-on losses 3

1.2 Soft switch-on method 4

1.3 Active recovery circuit 5

1.4 Passive recovery circuit 6

2 **The new ST solution - BC^2: energy recovery circuit 7**

2.1 Concept description 7

2.2 Phase timing description 8

2.2.1 Phase before t0 9

2.2.2 Phase t0 to t1 9

2.2.3 Phase t1 to t2 10

2.2.4 Phase t2 to t3 11

2.2.5 Phase t3 to t4 11

2.2.6 Phase t_4 to t_5 12

2.3 Electrical voltage stress in BC^2 13

2.4 Calculation of m2 and m1 ratios 13

2.5 Calculation of L 14

2.6 Range of products 14

3 **BC^2 design in 450 W PFC 15**

3.1 BC^2 design 15

3.2 BC^2 typical waveforms 15

3.3 Efficiency comparison 16

3.4 Thermal measurement 18

4 **Conclusion 19**

5 **References 20**

6 **Revision history 21**

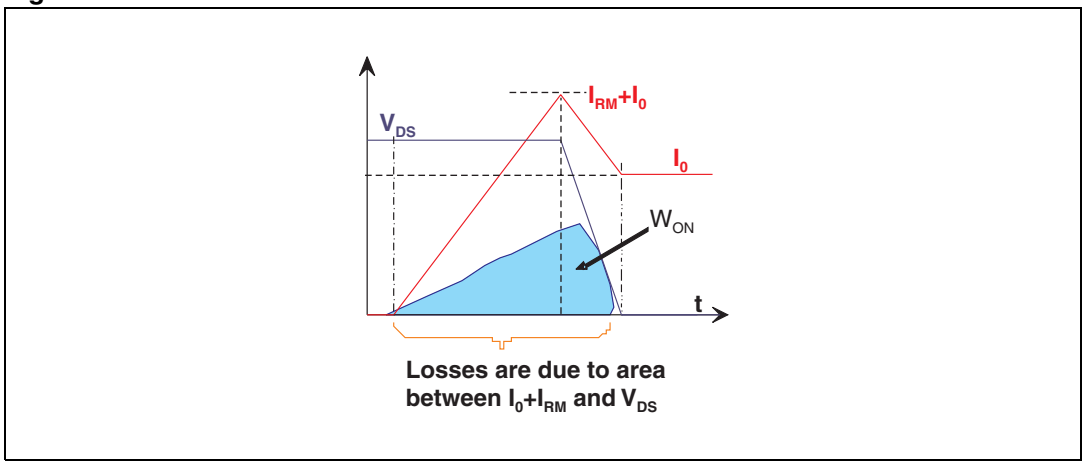
1 Existing solutions

This section describes some existing areas for efficiency improvements in PFC applications.

1.1 Diode switch-on losses

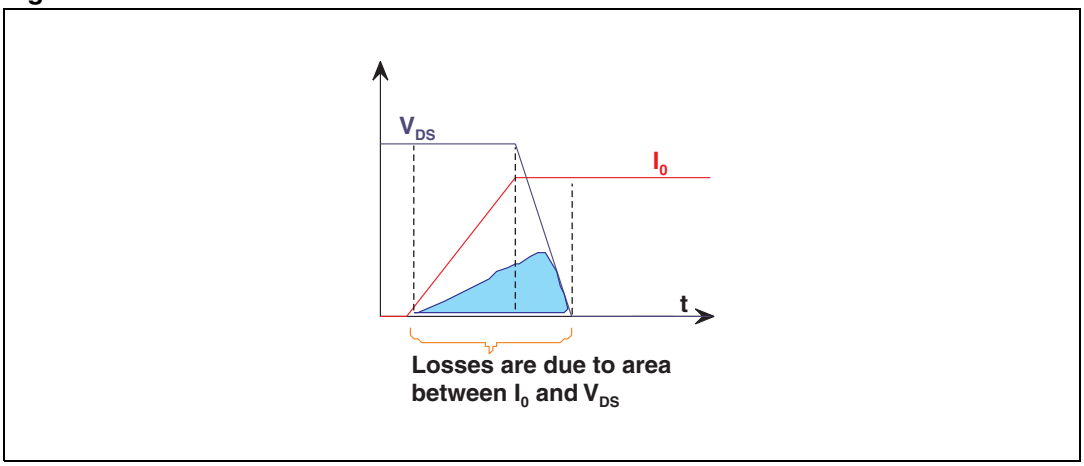
Usually, in mass market applications between 200 W and 2 kW, a power factor corrector (PFC) working in continuous conduction mode (CCM) is mandatory. To improve the power converter density, the switching frequency should be increased. Nevertheless, when the switching frequency increases, power dissipation in the power switch/rectifier commutation cells leads to the major switching losses in the PFC. The main power losses occur during turn-on of the power switch due to both the voltage and current crossing area of the MOSFET and the reverse recovery losses [see *Section 5: References*, *2.*] produced by the PN diode as shown in *Figure 1*.

Figure 1. Switch-on losses in PN diode behavior



To reduce the losses of the PN rectifier, many semiconductor manufacturers have recently introduced high-voltage Schottky diodes using SiC and GaN technologies. However, it is impossible to completely remove the voltage and current crossing area during transistor turn-on by improving component performance only.

Figure 2. Switch-on losses in SiC or GaN diode behavior

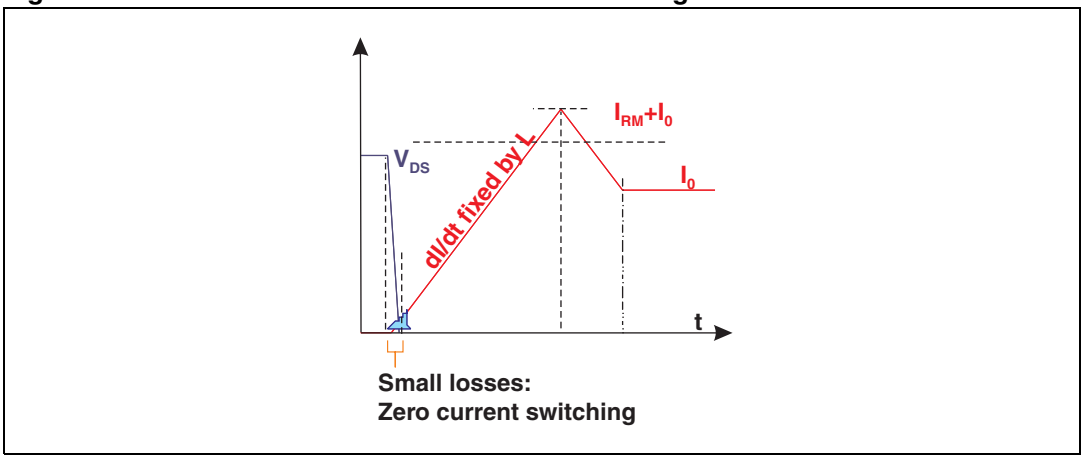


Unlike PN diodes, SiC diodes allow the turn-on dI/dt to be increased without increasing the diode recovery current. Thus, switching time decreases and switch-on losses decrease too, but they are not removed entirely. Today, in PFC designs, the turn-on dI/dt with the SiC diode is around 1000 A/µs maximum to respect EMI standards, whereas the PN diode is used with a dI/dt of 300 A/µs.

1.2 Soft switch-on method

Another way to reduce these losses is to use a soft switching method by adding a small inductor L to control the dI/dt slope. This solution removes the current/voltage crossing area and the PN diode recovery current effect during the turn-on of the transistor as shown in *Figure 3*.

Figure 3. Switch-on losses in current soft switching behavior



This soft switching solution is well known, but it requires that several technical criteria be met:

- Reset the current in the inductor L at each switching period, whatever the variations of the current, and input and output voltages.
- Recover the saved inductive energy without losses.
- Limit any overvoltage and overcurrent stress in the semiconductor devices.
- Keep cost down when adding any device.
- Maintain a similar power supply density.

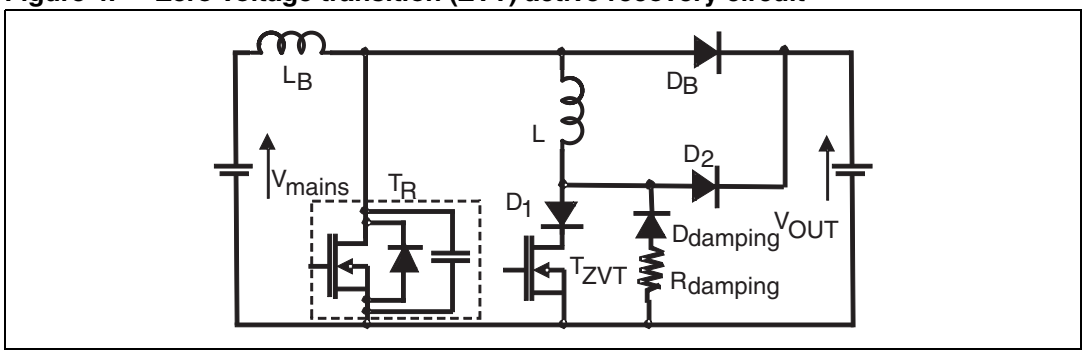
There are many circuits that are classified in two families of recovery circuits:

- active
- passive

1.3 Active recovery circuit

In the active recovery circuit family, the zero voltage transition (ZVT) [see *Section 5: References*, *3.*] shown in *Figure 4* is well known by designers. This circuit allows both switch-on and switch-off power losses to be removed.

Figure 4. Zero voltage transition (ZVT) active recovery circuit



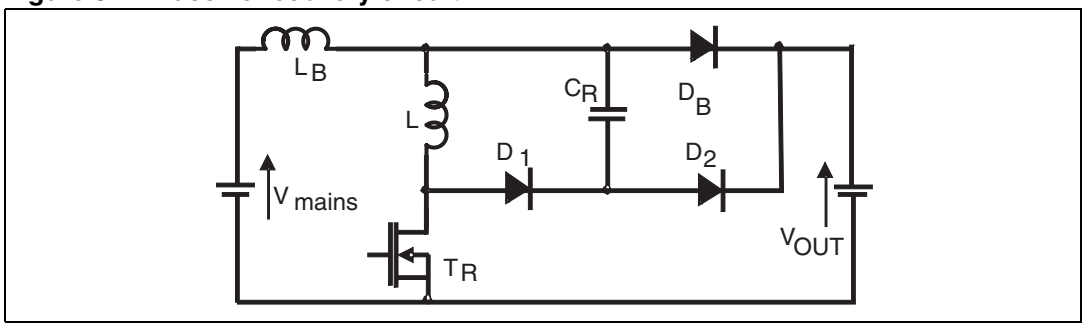
A theoretical study indicates that ZVT is an excellent topology for the PFC application, since all the switch losses are removed. In addition, this circuit can work whatever the input and output power variations. Nevertheless, in practice, the recovery current from the boost diode D_B significantly affects the ZVT behavior leading to some constraints on both inductance and minimum duty cycle. During the reset current in the small inductor L, the recovery current from D_2 involves a high-stress voltage and damping parasitic oscillation. Finally, the dynamic behavior of the PN diode affects the global ZVT efficiency because conduction times in the transistor should increase and a dissipative snubber is mandatory to reduce the electrical stress across the semiconductors.

In terms of cost the ZVT circuit requires an additional power MOSFET and a specific PWM controller. Several derivative circuits of the ZVT circuit have the same technical issue and their higher price makes these circuits less than ideal for mass market applications. Therefore, the passive recovery circuit can be more attractive.

1.4 Passive recovery circuit

In the passive recovery circuit family the electrical schematic shown in *Figure 5* is a good example [see *Section 5: References*, *4*.]; only two extra diodes and one resonant capacitor are required.

Figure 5. Passive recovery circuit



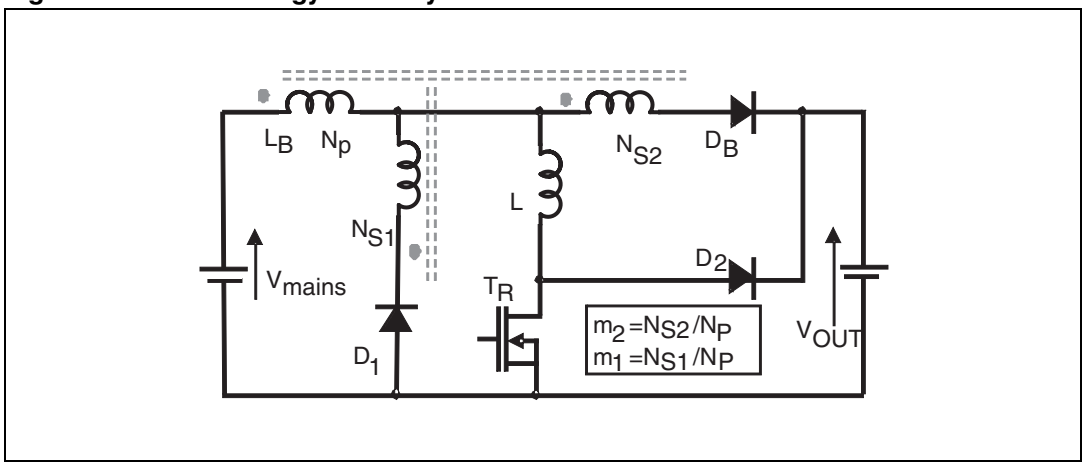
This circuit works well under unchanging external conditions. However, it is difficult to design this kind of system in PFC applications since the current reset in the small inductor depends on both boost diode recovery current and the external electrical conditions.

Although, the non-dissipative passive circuit requires fewer components, it is unfortunately technically impractical in PFC applications. These examples highlight that the current snubber method is well known but the technical challenge is to recover the L energy through the application without affecting the five criteria listed in *Section 1.2*.

2 The new ST solution - BC^2: energy recovery circuit

The innovative circuit has been designed [see *Section 5: References*, *1.*] to respect the five soft switching criteria in *Section 1.2*. *Figure 6* shows that two additional diodes D_1 and D_2 and two auxiliary windings N_{S1} and N_{S2} wound around the main boost inductor L_B are designed to reset the energy stored in the small inductor L.

Figure 6. Novel energy recovery circuit: BC^2

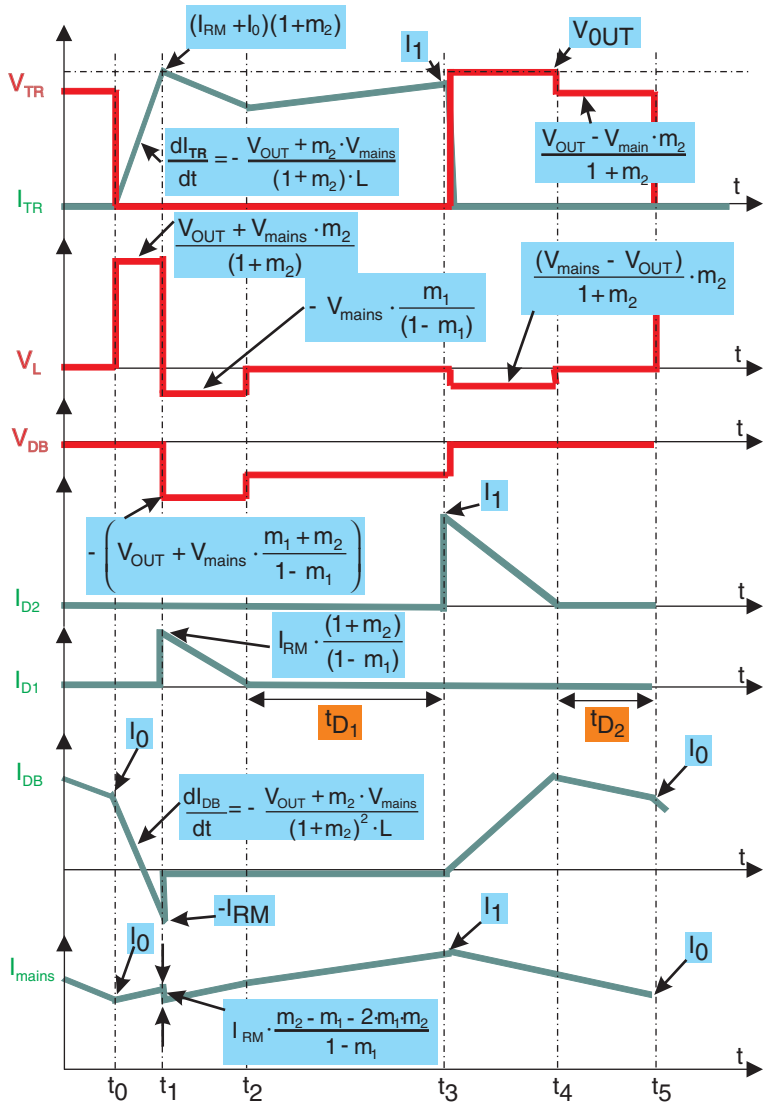


2.1 Concept description

The winding N_{S1} allows the I_{RM} current from the boost diode D_B to be recovered in the main boost inductor when the transistor turns on. Since the mains input voltage modulates the L_B voltage, it also modulates the reflected voltage across N_{S1}. This input voltage also modulates the boost diode current I_{DB} and its associated recovery current I_{RM}. These combined modulations allow the extra current I_{RM} flowing in the inductor L to be reset into the winding N_{S1} even in the worst case. The winding N_{S2} allows the extra current of L to be injected into the output capacitor when the transistor turns off. The reflected voltage across N_{S2} is also a function of the input voltage. This reflected voltage reaches its maximum when the AC line voltage is low, corresponding to the maximum value of the inductor L current. These combined variations allow the current flowing in the inductor L to be cancelled in the bulk capacitor through the diode D_2 even in the worst case. The benefits of these two additional windings N_{S1} and N_{S2} are to switch off the diodes D_1 and D_2 with a low dI/dt (about 10 A/µs) as in a discontinuous mode switching converter. Their recovery currents do not affect the behavior of the BC^2 circuit.

2.2 Phase timing description

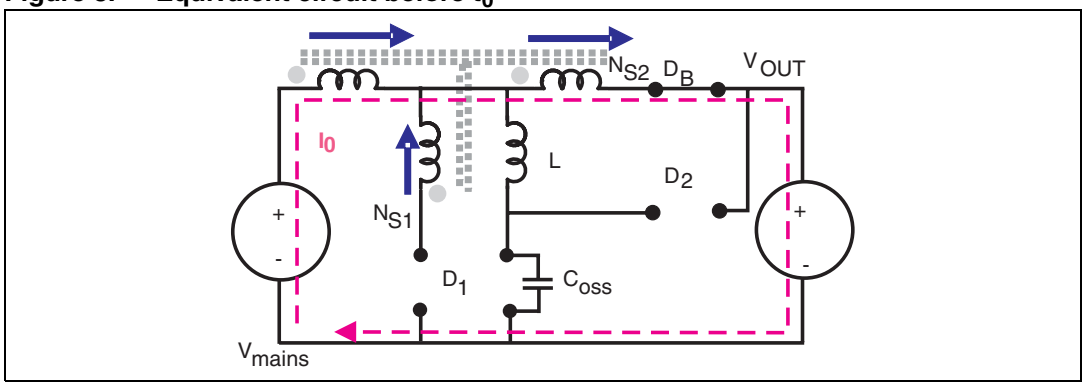
Figure 7. Equivalent timing per phase



The winding ratios m_1 and m_2 versus N_P winding are those of the windings N_{S1} and N_{S2} respectively.

2.2.1 Phase before t_0

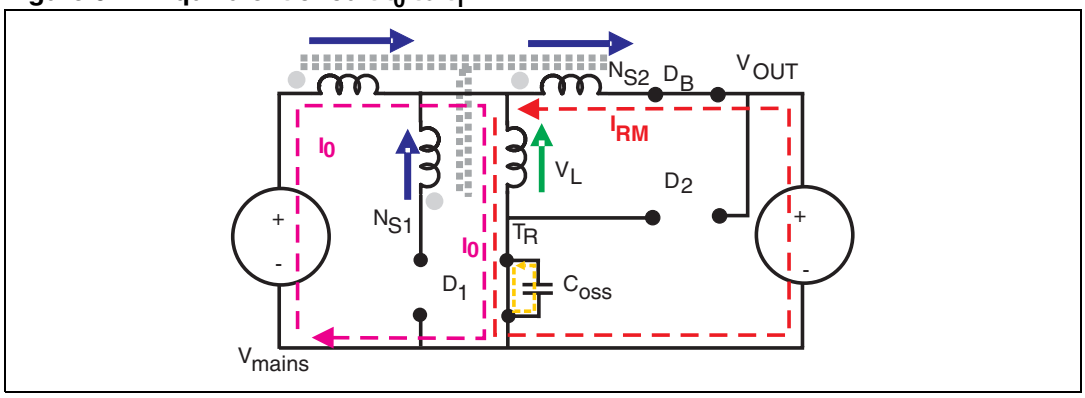
Figure 8. Equivalent circuit before t_0



Before t_0, the BC^2 circuit has the same behavior as the conventional boost converter. The boost diode D_B conducts to send the main inductor energy through the output bulk capacitor.

2.2.2 Phase t_0 to t_1

Figure 9. Equivalent circuit t_0 to t_1



At t_0, the power MOSFET turns on and the current in D_B is equal to I_0. At t_0+, the current soft switching occurs, that is to say, the voltage across the power MOSFET decreases to 0 volt under a zero current and no switching losses appear. After t_0, the current flowing in L increases linearly until it reaches the input current I_0 added with the recovery diode I_{RM}, whereas the current flowing in D_B decreases linearly down to $-I_{RM}$.

Figure 7 shows the behavior of these currents taking account of the m_2 transformer ratio. The simplified dI/dt expression in transistor T_R and the boost diode D_B can be estimated using,

$$\frac{dI_{DB}}{dt} \approx \frac{dI_{TR}}{dt} = \frac{V_{out} - V_{N_{S2}}}{L}$$

and

$$V_{N_{S2}} = \frac{(V_{out} - V_{mains}).m_2}{1+m_2}$$

At t_0 +, the C_{OSS} capacitance of the power MOSFET is discharged in its $R_{DS(on)}$. Unlike standard PFC circuits, the voltage applied across the drain is lower because the reflected

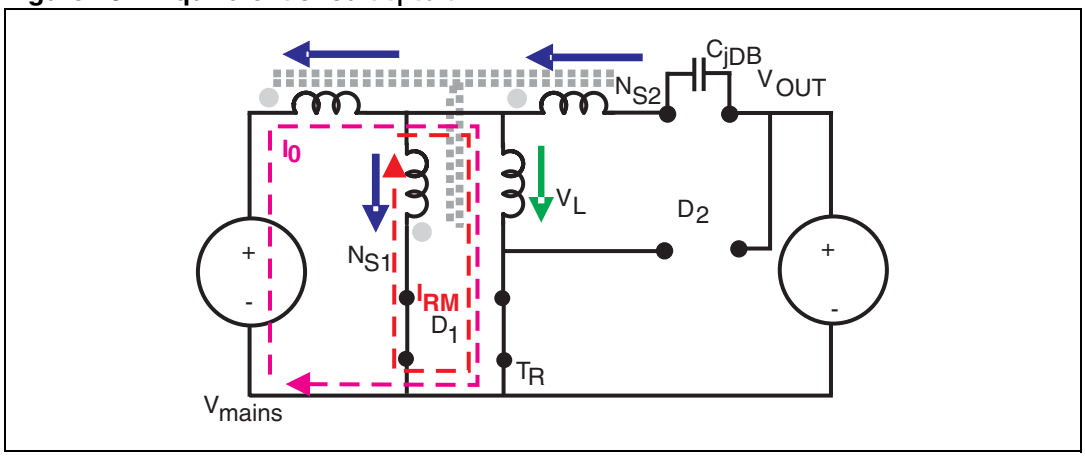
V_{NS2} voltage is subtracted from V_{OUT}. This behavior provides the BC^2 circuit with a benefit since under the low output load, power saving occurs in the system and it can be evaluated using:

$$P_{C_{OSS}-t_0} = \frac{1}{2}.C_{OSS}.\left[V_{out}^{\ 2} - \left(\frac{V_{out} + V_{mains}.m_2}{1+m_2}\right)^2\right].F_{switching}$$

Thus, the BC^2 reduces switch-off losses too.

2.2.3 Phase t_1 to t_2

Figure 10. Equivalent circuit t_1 to t2



At t_1+, the boost diode D_B turns off, and an overcurrent I_{RM} is stored in the small inductor. This overcurrent discharges the D_B junction capacitance linearly. At the same time, the voltage polarity across the main inductor changes until it reaches D_1 diode conduction. At this time, the overcurrent I_{RM} is reduced by the transformer ratio m_1 and is sent to the main inductor.

Thus, the current flowing through N_{S1} contributes to charge the internal coil magnetization L_B at the same time as the N_p winding biased by the mains voltage. The I_{RM} current flowing in D_1 decreases down to reach 0 A thanks to the reflected voltage V_{NS1} that it is given by:

$$V_{NS1} = \frac{-V_{mains}.m_1}{1-m_1}$$

and

$$t_{D1_ON} \approx \frac{I_{RM}.L.(1-m_1)}{V_{mains}.m_1}$$

To guarantee a soft switching behavior in discontinuous mode, the current in D_1 should reach 0 A before time t_3. The t_{D1_ON} time trend supports the PFC application since the I_{RM} current is the largest when the V_{mains} voltage in the sinusoidal period is the highest. In addition, to cancel the D_1 recovery current diode effect, the $dI/dt_{_D1}$ is always low thanks to the low reflected voltage V_{NS1} and it is given by:

$$\frac{dI_{_D1}}{dt} \approx \frac{-V_{mains}.m_1}{(1-m_1).L}$$

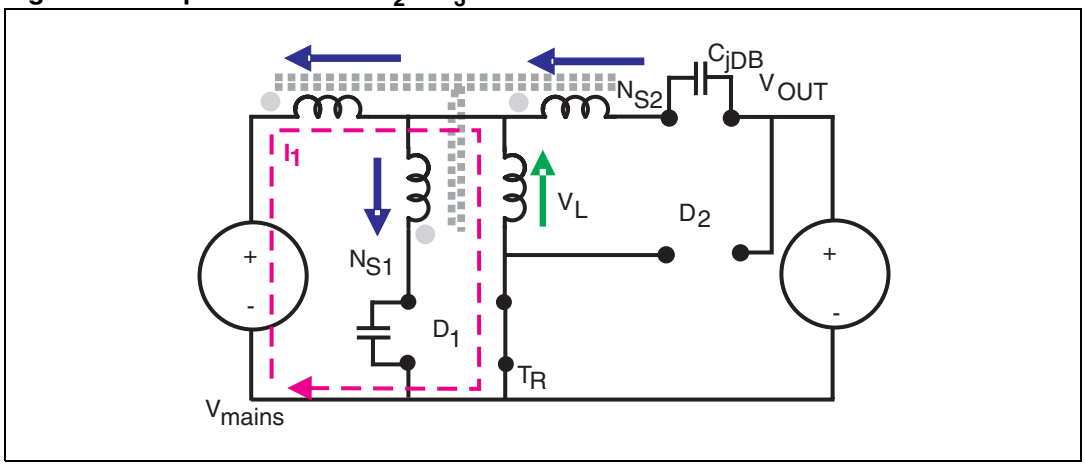
Unfortunately, during this phase a high reverse voltage is applied across the boost diode D_B:

$$V_{DB_reverse} = V_{out} + V_{N_{S1}} + V_{N_{S2}} = V_{out} + \frac{V_{mains}.(m_1+m_2)}{1-m_1}$$

This feature requires a specific diode for this application, so ST has developed an optimized diode with an accurate trade-off between the I_{RM} current value and its breakdown voltage.

2.2.4 Phase t_2 to t_3

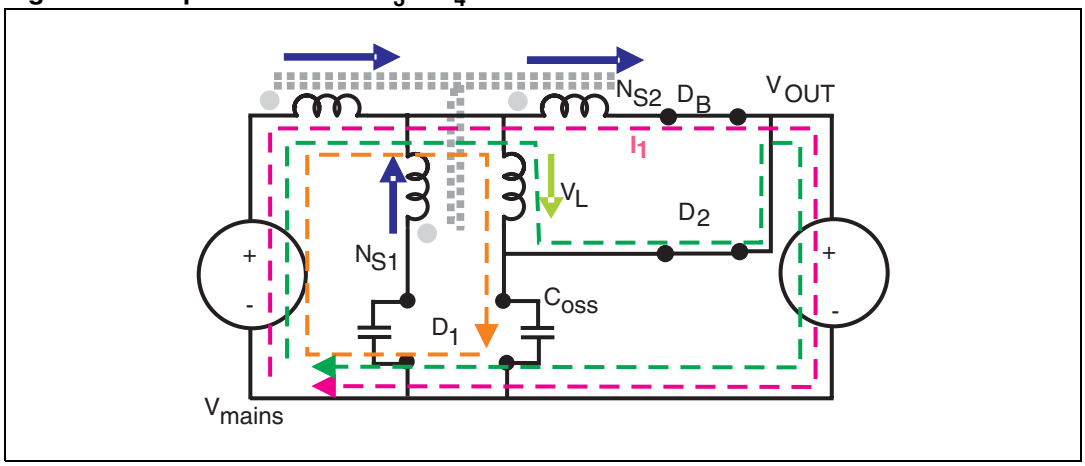
Figure 11. Equivalent circuit t_2 to t_3



At t_2, the current in D_1 reaches 0 A and then the BC^2 works as a conventional power boost converter. As the power transistor stays on, the current in the main L_B and the small L inductor increases up to I_1 at time t_3.

2.2.5 Phase t_3 to t_4

Figure 12. Equivalent circuit t_3 to t_4



At t_3, the power transistor turns off. At this time the voltage across the MOSFET increases linearly as its C_{OSS} capacitance is charged by the current stored in the small inductor L to reach conduction in diode D_2. No overvoltage stress occurs on the power switch during the turn off. At the same time, the voltage polarity across the main inductor changes until it reaches D_B diode conduction. As soon as the diodes conduct together, the output current is shared as shown in *Figure 7*. The current in D_2 starting at I_1, decreases due to the reflected voltage from N_{S2} to reach 0 A with a low dI/dt. On the other hand, the current in D_B rises to reach the nominal current at t_4. This shared current is a benefit for the BC^2 circuit. In the PFC application working under a lower mains voltage such as 90 V rms, the highest

application boost current is shared between D_B and D_1 diodes. Therefore the conduction losses in the rectification stage are reduced. The reflected voltage V_{NS2} and D_2 time conduction are given by:

$$V_{N_{S2}} = \frac{-(V_{out} - V_{mains}).m_2}{1+m_2}$$

and

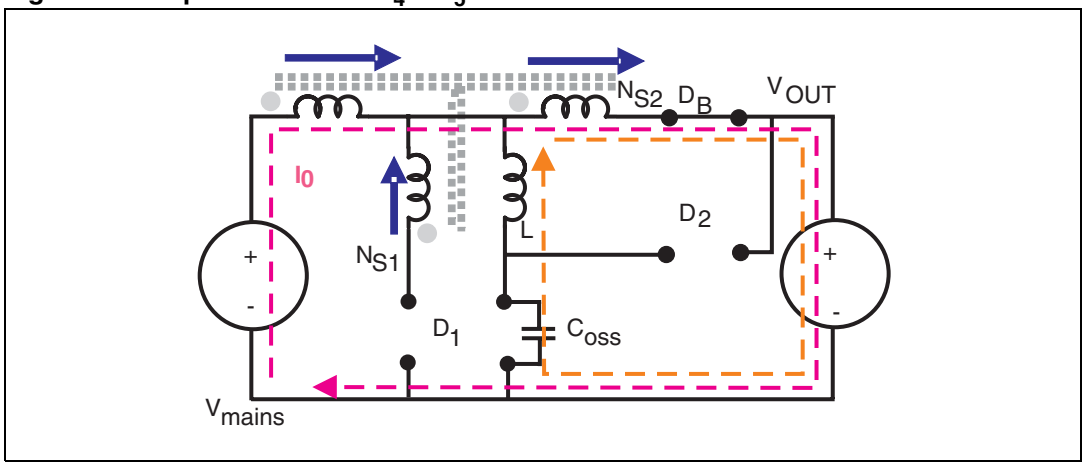
$$t_{D2_ON} = \frac{-I_1.L.(1+m_2)}{(V_{out} - V_{mains}).m_2}$$

The t_{D2_ON} time trend supports the PFC application since the I_1 current is largest when the V_{mains} voltage range is lowest. Thus the discontinuous mode could be guaranteed in the BC^2 circuit even under the worst case PFC applications such as high output load current under the minimum V_{mains} voltage range. In addition, to cancel the D_2 recovery current diode effect, the dI/dt_D_2 is always low due to the low reflected voltage V_{NS2} given by:

$$\frac{dI_D_2}{dt} \approx \frac{-(V_{out} - V_{mains}).m_2}{(1+m_2).L}$$

2.2.6 Phase t_4 to t_5

Figure 13. Equivalent circuit t_4 to t_5



At t_4, the current in the D_2 reaches 0 A and then the BC^2 works like a conventional power boost converter. Only the boost diode D_B conducts. Due to the reflected voltage of N_{S2}, the voltage across the power switch is lower than V_{OUT}. Thus the C_{OSS} capacitor is discharged in the bulk capacitor and power saving occurs as the transistor turns on at t_0.

2.3 Electrical voltage stress in BC^2

Table 1 summarizes the maximum voltage across each semiconductor versus the phases.

Table 1. Maximum reverse voltage in the BC^2

Maximum voltages	Phases	Waveform expression	> V_{OUT}?
VR_{TRmax}	t_3 - t_4	V_{OUT}	NO
VR_{DBmax}	t_1 - t_2	$\frac{V_{mainsRMSmax} \cdot \sqrt{2} \cdot (m_1 + m_2)}{1 + m_1} + V_{OUT}$	YES
VR_{D1max}	t_0 - t_1 t_3 - t_4	$\frac{(V_{mainsRMSmax} \cdot \sqrt{2} - V_{OUT}) \cdot (m_1 + m_2)}{1 + m_2} + V_{OUT}$	NO
VR_{D2max}	t_0 - t_1 t_1 - t_2 t_2 - t_3	V_{OUT}	NO

The BC^2 circuit needs to use a specific diode with a breakdown voltage higher than 600 V. Moreover, its recovery current should be optimized to avoid an higher current in the power transistor during the phase [t_1-t_2]. ST has developed specific diodes (STTH16BC065C, STTH10BC065C and STTH8BC065) for the BC^2 circuit. They have been designed to sustain average currents of 5 to 8 A (depending on the application) and a repetitive reverse voltage V_{RRM} of 650 V.

2.4 Calculation of m_2 and m_1 ratios

To respect the discontinuous operating mode during the timing phases [t_1-t_2] and [t_3-t_4], the time td1 and td2 shown in *Figure 7* should be always positive. According to the typical CCM PFC rules and both t_{D1_ON} and t_{D2_ON} expressions, it becomes easy to define the m_1 and m_2 transformer ratio conditions.

$$m_2 > \frac{P_{IN}\,max \cdot V_{OUT} \cdot L \cdot F_s}{V^2_{mainsRMS}\,max \cdot \left(V_{OUT} - V_{mainsRMS}\,max \cdot \sqrt{2}\right) - \left(P_{IN}\,max \cdot V_{OUT} \cdot L\right)}$$

and

$$m_1 > \frac{(1 + m_2) \cdot I_{RM}\,max \cdot L \cdot V_{OUT} \cdot F_s}{V_{mains}\,max \cdot \sqrt{2} \cdot \left(V_{OUT} - V_{mains}\,max \cdot \sqrt{2}\right)}$$

Where P_{IN} is the input PFC power, F_s is the switching frequency, $V_{mainsRMS}$max is the maximum rms voltage range and the I_{RM}max is the maximum current recovery under the turn-on dI/dt at its maximum operating junction condition.

2.5 Calculation of L

There are several ways to rate the inductance L. For instance, its turn-on dI/dt can be rated at 50 A/µs. Then, m_2 and m_1 are calculated taking into account the corresponding I_{RM} of diode D_B. However, the reverse voltage across the D_B, $V_{RDB_}$reverse, must not exceed 75% of V_{RRM} to meet the system design rule, 75% x 650 = 487 V. If $V_{RDB_reverse}$ is higher than 487 V, the L value should be reduced. Therefore, the dI/dt of L and the I_{RM} diode of D_B increase as well. Thus, m_1 and m_2 should be recalculated to get $V_{RDB_reverse}$ below 487 V. But this calculation method does not optimize the inductance L and its size. Ultimately, a good rating should minimize L size. ST has developed a software tool using all the parameters: the I_{RM} diode of D_B versus the dI/dt and junction T_J, the L inductance tolerances, and the switch-on power losses. This tool is proposed to help designers to choose the best L inductance for its application. *Table 2* shows two PFC examples using the BC^2 concept.

Table 2. Inductor and size versus the PFC types

	Case 1	Case 2
Input power	100 W < Pin < 1.1 kW	50 W < Pin < 450 W
V_{mains}RMS	90V < V_{mains}rms < 264 V	90 V <V_{mains}rms< 264 V
V_{OUT}	400 V	400 V
Fs	95 kHz	95 kHz
Inductor and size	3 µH	5 µH
Core reference	Core DR78381 (Datatronics Limited)	Core DR79124 (Datatronics Limited)

2.6 Range of products

ST offers the BC^2 technology in a range of products:

- STTH8BC065DI, STTH8BC060D, STTH5BCF060 for applications from 800 W to 2 kW
- STTH16BC065CT, STTH5BCF060 for applications from 400 W to 1 kW
- STTH10BC065CT + STTH3BCF060U for applications from 280 W to 600 W

3 BC^2 design in 450 W PFC

A universal line range 90 to 264 V_{mains} rms 450 W power factor corrector working in hard switch mode using a standard average current mode PWM has been developed to highlight the benefits of the BC^2 circuit. Switch-on behavior, efficiencies and thermal measurements have been compared with 8 A SiC Schottky diodes.

3.1 BC^2 design

Specific diodes have been used for the BC^2 circuit such as the STTH8BC065 for D_B, the STTH8BC060 for D_2 and the STTH5BCF060 for D_1 as shown in *Figure 6*. The software tool provides the L inductance, m_1 and m_2 versus the switching frequency as given in *Table 3*.

Table 3. N_{S1}, N_{S2} and L versus Fs

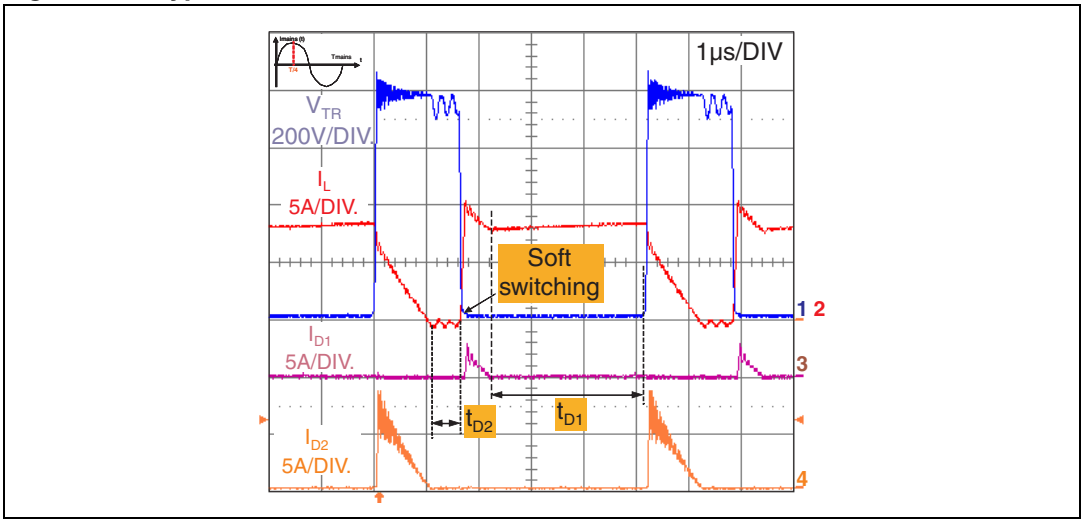
Fs	72 kHz	140 kHz	200 kHz
N_P	52 turns, L_B = 600 µH, Tore METGLAS 4520MPEC		
N_{S1}	2 turns	4 turns	5 turns
N_{S2}	8 turns	8 turns	5 turns
L	8 µH	5.1 µH	2.7 µH

3.2 BC^2 typical waveforms

Figure 14 shows the typical BC^2 waveforms corresponding to a PFC working at 200 kHz.

At each power MOSFET switch-on, soft current switching occurs. This curve highlights that D_1 and D_2 diodes always work in discontinuous mode; D_1 recovers the I_{RM} current from D_B whereas D_2 sends the current stored in L through the PFC bulk capacitor. As soon as D_2 turns off, the power voltage drain decreases as previously mentioned in the [t_0-t_1] and [t_4-t_5] phases and switch-off power losses are saved.

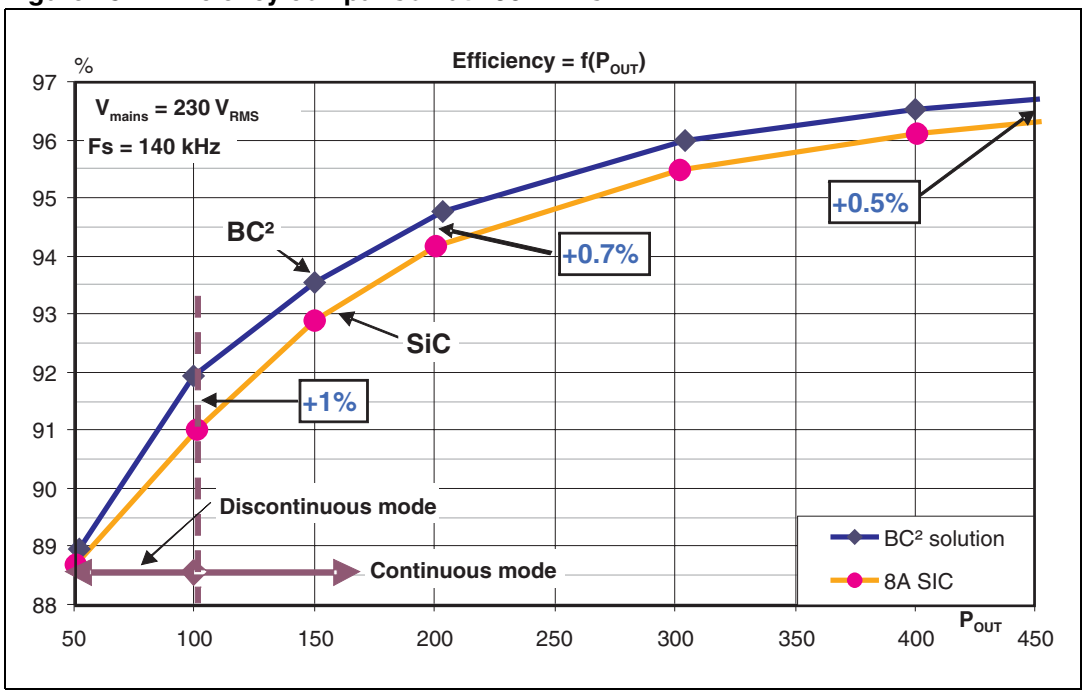
Figure 14. Typical BC^2 waveform at Fs = 200 kHz



3.3 Efficiency comparison

BC^2 and SiC diode efficiency have been compared under two V_{mains} levels as shown in *Figure 15* (230 V_{RMS}) and *Figure 16* (90 V_{RMS}) with a switching frequency equal to 140 kHz. At 230 V_{RMS}, the BC^2 circuit saves up to 2.25 W at full load and 1 W at 100 W compared to the 8 A SiC diode. Under low load, the reflected voltage from N_{S2} still improves the BC^2 efficiency because the switch-off losses are lower than the SiC as described in the phase time [t_0-t_1]. As soon as the PFC works in discontinuous mode (< 100 W) the SiC and the BC^2 have the same efficiency as shown in *Figure 15*.

Figure 15. Efficiency comparison at 230 V rms



At 90 V rms, the soft switching method benefits plus the power saving in the C_{OSS} discharge reinforces the benefit of the BC^2 circuit. Up to 5.4 W is saved thanks to the BC^2 at 450 W compared to the SiC diode and under low load, up to 1.7% is saved thanks to the switch-off power saving.

Figure 16. Efficiency comparison at 90 V rms

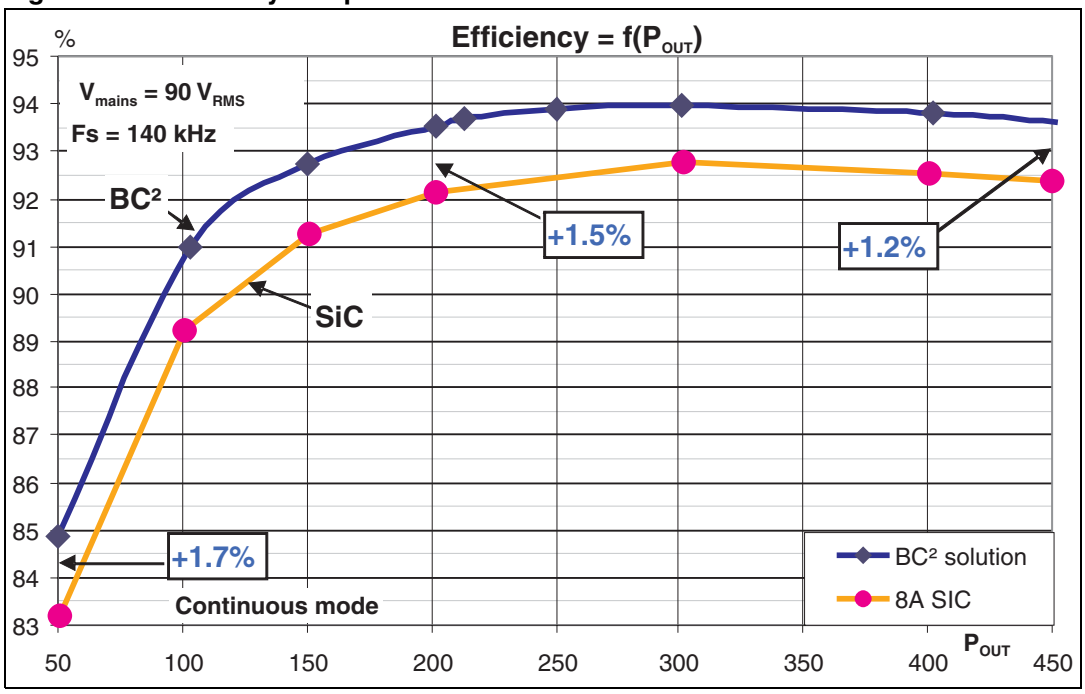


Figure 17. 450 W PFC efficiency versus three different output powers and three switching frequencies for V_{mains} rms = 90 V

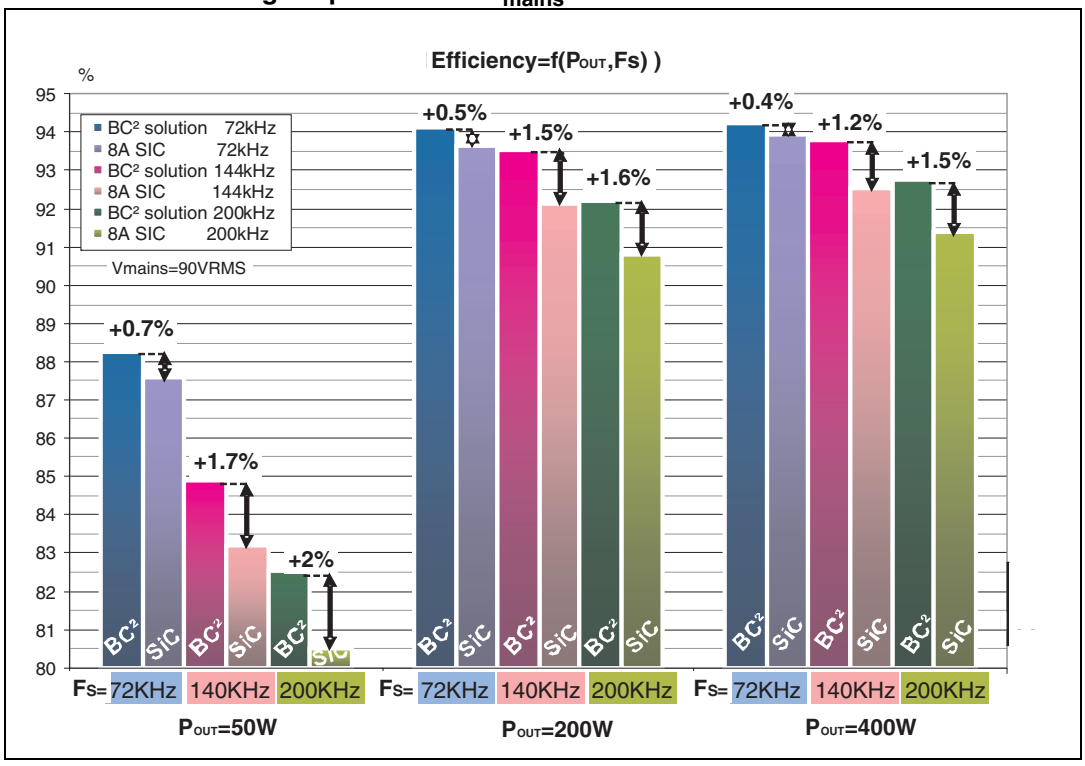


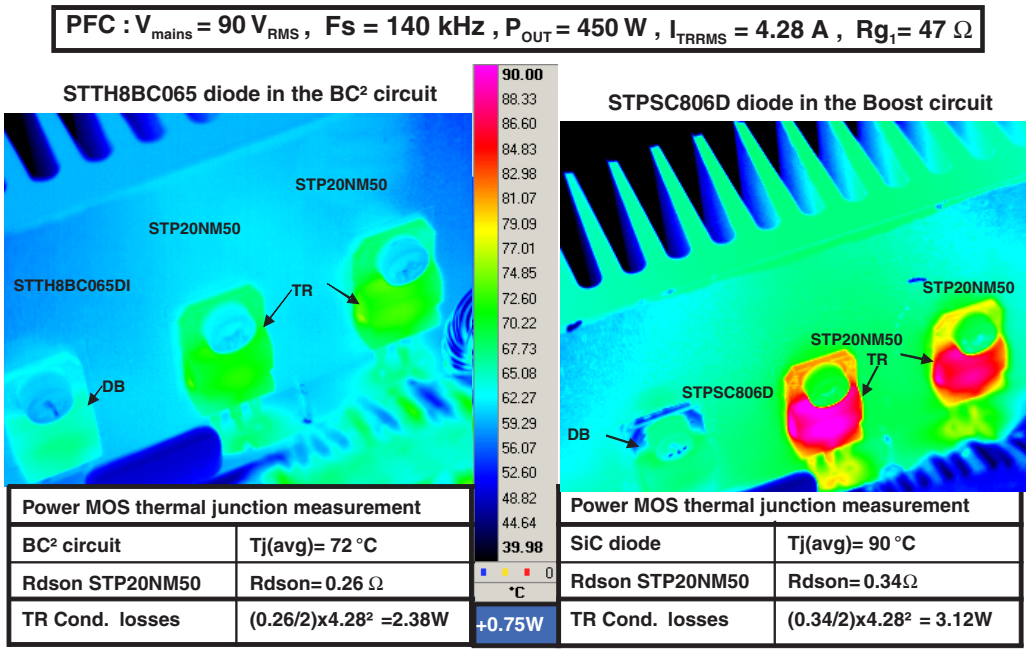
Figure 17 highlights the benefit of the BC^2 circuit soft switching method added to its C_{OSS} discharge power saving especially at low load.

3.4 Thermal measurement

The soft current switching method allows the power dissipation in the switch transistor to be reduced. *Figure 18* shows that a high thermal temperature difference (18 °C) occurs between the BC^2 and the SiC diode in the PFC application. For the same working junction temperature in the power transistor, the size of the thermal heatsink could be reduced. In this way, the space saving balances out the space from the small L inductor required by the BC^2 circuit. Therefore, the BC^2 circuit can have the same power density as the SiC diode solution. Nevertheless, the BC^{2}efficiency decreases due to the power MOSFET $R_{DS(on)}$ thermal rising. *Figure 18* shows that 0.75 W should be removed from the 5.4 W measured in the efficiency comparison at 90 V rms. Even in this configuration, the BC^2 circuit has a better efficiency than the SiC diode. The BC^2 circuit has a better power density and efficiency criteria than the SiC diode.

Another consideration is that, for the same thermal heatsink, the Power MOSFET size could be reduced to further reduce the PFC cost.

Figure 18. Thermal measurement comparison



4 Conclusion

The BC^2 circuit uses the soft switching method with a unique non-dissipative recovery circuit. STMicroelectronics has introduced the specific diodes suited for the BC^2 concept to improve the CCM PFC performance as shown in *Table 4*.

This circuit supports the actual energy efficiency recommendation at 20%, 50% and 100% of rated power supplies.

Table 4. BC^2 benefits in 450 W PFC, 140 kHz

Criteria at 90 V rms	SiC diode	BC^2 circuit	Benefits
Efficiency	92.5%	93.7%	+1.2%
Power MOSFET temperature	90 °C	72 °C	-18 °C
Power density at iso-efficiency	State of art	Improve, save 5.4 W	+1.2% gain
EMI	Acceptable with dI/dt < 1000 A/µs	Acceptable with dI/dt < 100 A/µs	Soft switching
Boost rectification cost	> 0.2 € per 100 W	>> 0.2 € per 100 W	Mass market

5 References

1. Benoît Peron, “Auxiliary switching circuit for a chopping converter”, Patent No: US 6,987,379 B2, June 2006
2. Bertrand Rivet, “New Solution to Optimize Diode Recovery in PFC Boost Converter”, PCIM 2000.
3. Jim Noon, UC3855A/B High Performance Power Factor Preregulator -Texas Instrument- application report- SLUA146A
4. Brian T, Irving and M. Jovanovic “Analysis, Design and Performance Evaluation of Flying-Capacitor Passive Lossless Snubber applied to PFC Boost Converter”, APEC 2002, pp. 503 - 508 vol.1.

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
10-Nov-2010	1	Initial release.

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